Please cancel claims 3, 4, 7 and 8 without predjudice.

Please amend the claims as follows:

(Amended) 1. A method of manufacturing a semiconductor device comprising a plurality of multi-voltage level MOS transistors comprising:

providing a semiconductor substrate having a plurality of active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto said plurality of active regions;

forming an electrode layer onto said gate oxide layer;

patterning said electrode layer to form a gate electrode onto each of said plurality of active regions:

oxidizing a sidewall of said gate electrode to form on said oxide layer a second thickness greater than said first thickness from said sidewall of the gate electrode towards a centre portion thereof;

doping said plurality of active regions at a first concentration with an impurity of a second conductivity type which is opposite to said first conductivity type using said gate electrode as a mask to form a first transistor driven at a first voltage level;

forming spacers on said sidewall of said gate electrode;

masking a portion of said plurality of active regions; and

doping an unmasked portion of said plurality of active regions at a second concentration higher than the first concentration with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level.